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EXAMINER	
JACOBSON, TONY M	

ART UNIT	PAPER NUMBER
2644	13

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/007,763	LI ET AL.	
	Examiner	Art Unit	
	Tony M Jacobson	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 8 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant has not disclosed an embodiment wherein the second low-pass filter (372 of Fig. 4) is coupled to combining circuitry along with the fifth low-pass filter (410) to produce the left-channel signal and right-channel signal. It appears that Applicant intended to recite, "said sixth low-pass filter" at line 7 of the marked-up claim, consistent with other portions of the current amendment, rather than "said second low-pass filter." The following prior-art rejection of this claim follows this assumption.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 1 recites a first low-pass filter at line 3 and a second low-pass filter at line 13, and then at line 16 recites "the output of said filter." Since two distinct filters were previously claimed, it is not evident to which "said filter" reference is being made.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-6, 8-13, 16-19, and 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vogt et al. (US 5,442,709) in view of Reich (US 4,827,515) and Kawamura (US 5,202,925).

8. Regarding claims 1, 18, 21, and 25, Vogt et al. discloses in Fig. 1, a decoder having an input signal (1) with a predetermined frequency (the sampling frequency, the frequency of a pilot signal component, and the frequency of a suppressed 38 kHz subcarrier are all predetermined, as in Applicant's invention; other varying, non-predetermined frequency components are also present, as in any conventional FM stereo multiplexed signal) and a first output signal (13), comprising a multiplier (15 or 15a) for multiplying a predetermined value (16) by the input signal to generate an intermediate signal, wherein the input signal has a pilot signal component and wherein the pilot signal component in the intermediate signal is a predetermined lower frequency

than the pilot signal component in the input signal (see column 4, lines 20-36); a ("second") low-pass filter means (18 and 17) for receiving the intermediate signal and providing the pilot signal as an output; a phase angle estimation means (21 – see Fig. 2) for receiving the pilot signal component (SPC1 or SPC2) from the output of said [second] filter, said phase estimation means determining an approximate phase of the pilot signal component of the input signal and generating at least one trigonometric function (G38c and G38s) using the approximate phase of the pilot signal component of the intermediate signal (see column 4, line 18 -column 5, line 18); quadrature mixer means (2, 3, and 14) coupled to the input signal for shifting the input signal from the predetermined frequency to a lower frequency by forming a pair of quadrature signals (column 3, lines 18-56); means (4 and 5 of Fig. 1) for using the at least one trigonometric function (G38c, G38s), the first quadrature mixer output (Imr1), and the second quadrature mixer output (Imr2) to generate a phase-aligned output signal (L-R, at 6) that contains a difference of the left channel information and the right channel information; and means (7-11) for using the output signal that contains a sum of left channel information and right channel information and using the output signal that contains a difference of left channel information and right channel information to generate a left channel signal (12) and a right channel signal (13). Vogt et al. does not disclose a "first" low-pass filter for low-pass filtering the input signal to provide a "first" filter output; a "first" decimator coupled to the "first" low-pass filter for decimating the "first" low-pass filter output to reduce a sampling frequency of the input signal, the "first" decimator providing an output signal that contains a sum of left channel information and

right channel information; a "third" low-pass filter and a "fourth" low-pass filter for low-pass filtering each of the pair of quadrature signals; a "second" decimator coupled to the "third" low-pass filter for decimating a first of the pair of quadrature signals to provide a first quadrature mixer output; a "third" decimator coupled to the "fourth" low-pass filter for decimating a second of the pair of quadrature signals to provide a second quadrature mixer output; nor that the means for using the output signal that contains a sum of left channel information and right channel information and using the output signal that contains a difference of left channel information and right channel information to generate a left channel signal and a right channel signal comprises a "fifth" low-pass filter and a "sixth" low-pass filter that are dynamically and separately controlled low-pass filters, the "fifth" low-pass filter processing the output signal that contains sum of left channel information and right channel information and having its bandwidth varied after first varying bandwidth of the "sixth" low-pass filter that processes the output signal containing a difference of left channel information and right channel information, an amount of bandwidth adjustment depending upon received signal conditions. Although Vogt et al. does not disclose low-pass filters filtering the input signal and the pair of quadrature signals output by the quadrature mixer means nor "first", "second", or "third" decimators coupled to the filter means for decimating the filtered input signal, first quadrature signal, and second quadrature signal, respectively, Vogt et al. does disclose low-pass filters 17 and 18 and corresponding decimators 19 and 20 low-pass filtering and decimating the pair of quadrature signals produced by the multipliers 15 and 15A, wherein the pilot signal component in the intermediate signal is a lower frequency than

the pilot signal component in the input signal. Vogt et al. discloses at column 4, lines 33-40 that because the frequency of the frequency-reduced quadrature pilot signals output from the multipliers (15 and 15A) (less than about 70 Hz) is much lower than that of the original pilot frequency, the sampling rate is reduced at decimators 19 and 20, which saves significant expense in the following network (21). Reich discloses a similar FM stereo demodulator (decoder) in Fig. 1, in which the various signals are low-pass filtered and decimated at several points in the circuit. Specifically, the composite input signal is low-pass filtered and decimated at d1 by a factor of "M" to reduce the input sampling rate to 228 kilo-samples per second (kS/s); the resulting signal is further reduced in sampling rate by a factor of 3, to 76 kS/s at d2 to form a reduced-rate composite signal, and the difference signal is low-pass filtered and decimated by a factor of 3 at d3 after having been mixed with a phase-aligned carrier at the frequency of the suppressed carrier of the difference signal component of the composite signal at multiplier m3. Reich discloses at column 1, line 58 –column 2, line 3, "As is well known, the reduction of the sampling rate has the advantage of reducing the clock frequency of following subcircuits, so that the digital filter circuits can be constructed with fewer stages and require correspondingly less area on an integrated circuit chip. Therefore, it is advantageous to adapt the sampling rate to the maximum useful signal frequency to be processed. The sampling rate must not be lower than twice the value of the useful signal frequency, however. As a rule, each decimation circuit includes a filter portion, which prevents aliasing during decimation." (a low-pass filter preceding the decimator, as is well-known in the art) Reich further discloses at column 2, lines 49-55, "The

sampling frequency of the signals provided at the outputs of the first and second demodulators m1, m2 is very high compared with the frequency of these signals, which is practically zero, so that the sampling rate after the first and second demodulators m1, m2 should be greatly decimated". Kawamura discloses in Fig. 3, an FM stereo receiver having an improved automatic reception control (ARC) system and method. Kawamura discloses that the circuit improves on the prior-art circuit of Fig. 7, which has, as part of means for using a signal that contains a sum of left-channel information and right-channel information (main signal S_M) and using a signal that contains a difference of left-channel information and right-channel information (sub-signal S_S) to generate a left-channel signal and a right-channel signal (S_L and S_R), a variable high-cut (low-pass) filter (2) under the control of high-cut control circuit (8) dynamically controlling the bandwidth of a main signal S_M (containing a sum of left-channel information and right-channel information) controlling the high-frequency content of that signal in response to received signal conditions (signal strength) and a variable attenuation circuit (3) under the control of separation control circuit (3A) dynamically controlling the amplitude of a sub-signal S_S (containing a difference of left-channel information and right-channel information) in response to received signal conditions (signal strength). (See column 1, lines 8-42.) The improvement is made by substituting a second high-cut (low-pass) filter (5 of Fig. 3) for the variable attenuation circuit (3) of Fig. 7, still under the dynamic control of a separation control circuit (now 5A). (See column 2, lines 15-23.) Kawamura discloses at column 1, lines 60-64 that the separation control is effected when the received signal strength level is within the range of, for instance, from 45

dBμV to 25 dBμV (decibels referenced to 1 microvolt), whereas the frequency control is carried out when the received signal strength is less than 35 dBμV. Thus, the improved circuit of Fig. 3 comprises a first ("fifth") high-cut (low-pass) filter (2) and a second ("sixth") high-cut (low-pass) filter (5) that are dynamically and separately controlled low-pass filters, the first ("fifth") low-pass filter processing the (output) signal that contains a sum of left-channel information and right-channel information and having its bandwidth varied after first varying bandwidth of the second ("sixth") low-pass filter that processes the output signal containing a difference of left-channel information and right-channel information, an amount of bandwidth adjustment depending upon received signal conditions. (For a decreasing signal strength, separation control 5A will reduce the bandwidth of the second ("sixth") low-pass filter (5) when the signal strength reaches a level of 45 dBμV; then, after the signal strength is further reduced to a level below 35 dBμV, high-cut control circuit 8 will reduce the bandwidth of the first ("fifth") low-pass filter (2) as described at column 1, lines 60-64.) Kawamura discloses at column 2, lines 9-13 that the improved circuit provides the advantage that stereo separation is maintained, even under low field-strength conditions. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to apply the teachings of Reich to the decoder of Vogt et al. by providing a "first" low-pass filter and a "first" decimator for low-pass filtering and decimating the input signal prior to application to adder and subtractor processing stages 8 and 9, with the "first" low-pass filter and "first" decimator configured to pass the bandwidth of the desired baseband audio (typically 15 kHz, as is well known in the art) at an appropriate sampling rate; and

"third" and "fourth" low-pass filters and "second" and "third" decimators to low-pass filter and decimate the pair of quadrature signals output by the quadrature mixer means (2, 3, and 14) for low-pass filtering and decimating the first quadrature signal and second quadrature signal, respectively, with the "third" and "fourth" low-pass filters and "second" and "third" decimators configured to pass the bandwidth of the difference-frequency components of the pair of quadrature signals (which is the same as that of the baseband audio signal in a standard FM multiplex stereo signal, 15 kHz, as is well known in the art) at a sampling rate of at least twice the frequency of this bandwidth (at least 30 kHz) in order to reduce the computational burden and expense of the following stages while passing all the desired signals without aliasing. It would have also been obvious to further modify the decoder of Vogt et al. by providing dynamically and separately controlled "fifth" and "sixth" low-pass filters to vary the bandwidth of the demodulated audio signals, operating upon the sum and difference signals, respectively, depending upon received signal conditions according to the teachings of Kawamura, in order to provide a decoder that can be implemented with minimum expense while minimizing the effects of received noise with minimal loss of desired high frequency content and stereo separation. (In this and the following rejections, the use of quoted numbers, such as "first", "third", etc., in referring to elements of the prior art indicates correspondence to the language of Applicant's claims, not to a count of such elements in the prior art; e.g., although a prior art reference may teach only two filters, one of those may be referred to as a "fourth" filter, in order to make clear the

correspondence to a "fourth filter" recited by Applicant.)

9. Further regarding claim 18, the decoder of Vogt et al., modified according to the teachings of Reich and Kawamura as described above, performs the method claimed in normal operation. (See also Vogt et al. column 1, lines 35-43.)

10. Further regarding claim 21, the decoder of Vogt et al., modified according to the teachings of Reich and Kawamura as described above, performs the method claimed in normal operation. The "predetermined frequency" recited is not further specified in the claims; and the frequency of a pilot signal component, and the frequency of a suppressed 38-kHz subcarrier, present in the input signal of the decoder of Vogt et al. as well as that of Applicant, are both predetermined and are both shifted from their respective predetermined frequencies to lower frequencies (and also shifted to higher frequencies, since the mixing processes at multipliers 2 and 3 of Vogt et al. produce sum and difference frequencies) in the process of forming the pair of quadrature signals Imr1 and Imr2.

11. Regarding claim 2, Vogt et al. discloses at column 3, lines 66-67 that the at least one trigonometric function (G38s and G38c) includes a sine function and a cosine function.

12. Regarding claims 3 and 4, Vogt et al. discloses in Fig. 1 and at column 4, lines 18-26 that the predetermined value at multiplier (15) is a cosine value retrieved from a table (16).

13. Regarding claim 5, in the decoder of Vogt et al., modified according to the teachings of Reich and Kawamura as described above regarding claim 1, the useful bandwidth of each of the low-pass filtered and decimated signals from the "first", "second", and "third" decimators are all substantially 0-15 kHz; therefore, it would have been obvious to one of ordinary skill in the art at the time the present invention was made to low-pass filter each of the three signals to this bandwidth and decimate them accordingly to the same sampling rate, according to the teachings of Reich as described above regarding claim 1 and also in view of the fact that these signals must be combined at 6, 8, and 9, which requires equal sampling rates.

14. Regarding claim 6, the decoder of Fig. 1 of Vogt et al., modified according to the teachings of Reich and Kawamura as described above regarding claim 1, further comprises a "fourth" decimator (19 or 20 of Fig. 1 of Vogt et al.) coupled between the "second" low-pass filter (17 or 18) and the phase angle estimation means (21), decimating the (frequency-reduced) pilot signal component (column 4, lines 18-40).

15. Regarding claim 16, in the system of Vogt et al., modified according to the teachings of Reich and Kawamura as described above regarding claim 1, although the

basic teaching of Reich at column 1, lines 58-66 suggests that the sampling frequency could be reduced as low as 140 S/s in view of the bandwidth of filters 17 and 18 (70 Hz) as described at column 4, lines 26-36 of Vogt et al., one of ordinary skill in the art would recognize that a significantly higher sampling rate would be preferred in order to convey the necessary phase angle information required to provide a relatively smooth phase correction (phase rotation) of the quadrature pair of signals Imr1 and Imr2 at multipliers 4 and 5. A sampling frequency range of about 4 to 100 times the expected maximum output frequency of the phase angle estimation circuit (21) (140 Hz, since circuit 21 doubles the input frequency) would seem reasonable, corresponding to a sampling frequency range of about 560 S/s to 14 kS/s. Given the disclosed input sampling rate of 228 kS/s in the decoder of Vogt et al., this corresponds to a sampling rate decimation factor in the range of 16 to 407. The obviousness or advantage of any particular decimation factor depends directly upon the initial sampling rate, which is not specified in the claims of the current invention. Since the decimation factor required to achieve a desired target sampling rate depends upon the sampling rate of the applied input signal, it would have been obvious to one of ordinary skill in the art at the time the present invention was made to select any appropriate sampling rate decimation factor to provide a suitable phase angle resolution in the phase angle estimation means (21) depending upon the sampling rate of the applied input signal. Given the input sampling rate of 228 kS/s, specified by Vogt et al. and Reich, a conservative factor of 20 would be reasonable, and selecting such a factor would have been obvious to one of ordinary skill

in the art at the time the present invention was made.

16. Regarding claim 8, in the decoder of Vogt et al., modified according to the teachings of Reich and Kawamura as described above regarding claim 1, the means for using the sum and difference signals comprises combining circuitry (7, 8, and 9 of Vogt et al., equivalent to stereophonic demodulation circuit 4 of Kawamura), coupled to the "fifth" low-pass filter (first high-cut filter 2 of Kawamura) and the "sixth" low-pass filter (second high-cut filter 5 of Kawamura), said combining circuitry combining the "fifth" low-pass filter output and the "sixth" low-pass filter output to produce the left and right channel signals; and control circuitry (high-cut control circuit 8 and separation control circuit 5A of Kawamura) coupled to the "fifth and the "sixth" low-pass filters for modifying bandwidth of the "fifth" low-pass filter and the "sixth" low-pass filter in response to received signal conditions. Vogt et al. discloses at column 5, lines 18-28 that the control circuitry (22), which modifies the amplitude of the difference signal to reduce stereo separation and also noise in response to received signal conditions in the original decoder may be constructed according to the disclosure of U.S. Patent application Ser. No. 08/215,186 (now US Patent No. 5,673,324 to Kässer et al.), incorporated by reference in Vogt et al. The circuit disclosed in Fig. 1 of Kässer et al. includes a symmetry detector (11) which detects asymmetry in the 38-kHz DSBSC (double-sideband suppressed-carrier) modulated difference signal and a high-pass detector (10) which detects high-frequency distortion caused by conditions such as multipath reception and, according to the detection of these conditions, influences an output

signal "D" at 26 to indicate a reduced quality of the received signal. Official notice is taken that it was well known in the art at the time the present invention was made that adjacent channel interference in a received FM signal typically causes a lack of symmetry between the received subcarrier sidebands of the received signal. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to utilize the more advanced control circuitry of Kässer et al. to implement each of high-cut control circuit 8 and separation control circuit 5A, rather than the simple RF signal strength detector circuits taught by Kawamura, in the decoder of Vogt et al., modified according to the teachings of Reich and Kawamura in order to provide a decoder with an automatic reception control that is responsive to the presence of adjacent signal interference and distortion of the input signal, rather than simply RF signal strength.

17. Regarding claims 9 and 10, Official notice is taken that the use of finite impulse response (FIR) filters in digital signal processing systems was notoriously well known in the art at the time the present invention was made, the corresponding counterpart filter classification being infinite impulse response (IIR) filters. It was further well known to modify the response characteristics (such as bandwidth) of an FIR by varying the filter coefficients. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to implement the variable-low-pass filters as taught by Kawamura as FIR filters in the decoder of Vogt et al., since the system is implemented as a digital signal processor (column 5, lines 32-38), and to modify the bandwidths of

the filters by varying the filter coefficients as was common in the art.

18. Regarding claim 11, Vogt et al. disclose that the system is used for decoding a multiplex signal in a stereo receiver of VHF/FM stereo broadcasting (column 1, lines 18-23 and column 3, lines 3-6).

19. Regarding claims 12 and 13, the predetermined value of Vogt et al. is nominally 19 kHz, the same as the nominal frequency of the pilot signal component in the input signal; however since it is independently generated in a free-running oscillator, it is approximate to, but not equal to, a frequency of the pilot signal component in the input signal and within 3 kHz (probably within a few Hz) of the frequency of the pilot.

20. Regarding claim 17, in the system of Vogt et al., modified according to the teachings of Reich and Kawamura as described above regarding claim 1, the phase angle estimation means (21) operates at a frequency less than one tenth a frequency of the input frequency. (The frequency-reduced pilot is nominally at 0 Hz, probably a few Hz at maximum, which is less than one tenth the predetermined frequency of the pilot at the input, 19 kHz; and the sampling frequency would be reduced as low as 140 S/s according to the teachings of Reich (column 1, lines 58-66), in view of the bandwidth of filters 17 and 18, 70 Hz, as described at column 4, lines 26-36 of Vogt et al., which is less than one tenth the predetermined sampling frequency of the input signal, 228 kS/s).

21. Regarding claim 19, Vogt et al. does not teach adding a predetermined phase correction to a phase value of the intermediate signal to produce a resultant phase value, wherein the predetermined phase correction is a function of a delay of a portion of the digital circuitry. Reich discloses at column 5, lines 20-41 and in Fig. 3 a circuit for adding a predetermined phase correction to a phase value of the frequency-reduced pilot signal quadrature pair of signals (equivalent to the intermediate signals SPC1 and SPC2 in Fig. 1 of Vogt et al.) to compensate for (as a function of) unequal delays introduced relative to other signals in the system. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to apply the teachings of Reich to the decoder of Vogt et al. by providing a circuit (or equivalent computations in a DSP) as shown in Fig. 3 of Reich, applied to intermediate signals SPC1 and SPC1 in order to provide a correct phase relationship between the quadrature pair of signals (Imr1 and Imr2) and the correction signals (G38c and G38s) despite unequal delays imparted upon these signals by their individual processing paths.

22. Regarding claim 22, Vogt et al. does not disclose the particular implementation of the filters in the decoder. Official notice is taken that the use of finite impulse response (FIR) filters in digital processing systems was notoriously well known in the art at the time the present invention was made, the corresponding counterpart filter classification being infinite impulse response (IIR) filters. FIR filters are often preferred over IIR filters because they have linear phase responses and are always stable (with symmetrical

coefficients), whereas IIR filters are not guaranteed stable and never have linear phase responses. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to implement the filtering processes in the decoder of Vogt et al, modified according to the teachings of Reich and Kawamura as described above regarding claim 21, as one or more FIR filters, since the system is implemented as a digital signal processor (column 5, lines 32-38).

23. Regarding claim 23, Vogt et al. discloses at column 5, lines 32-38 that the decoder may be implemented by suitable programming (in software, inherently) of a digital signal processor; thus, the filtering would be performed in software.

24. Regarding claim 24, in the software programmed DSP system of Vogt et al., modified according to the teachings of Reich and Kawamura as described above regarding claim 21, the filter coefficients would inherently be software modifiable.

25. Claims 14, 15, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vogt et al. (US 5,442,709) in view of Reich (US 4,827,515) and Kawamura (US 5,202,925) as applied to claims 1 and 18 above, and further in view of Patel et al. (US 5,479,449) and Whikehart et al. (US 5,936,438).

26. Regarding claims 14, 19, and 20, as described in previous Office actions, the basic function of the phase angle estimation circuit (21) of Vogt et al. is to receive a quadrature pair of signals (SPC1 and SPC2) representing the error between the phase and frequency of the reference pilot signal generated from table 16 with respect to the pilot component of the received signal and to generate a quadrature pair of output signals having frequency and phase equal to twice those of the input error signals (SPC1 and SPC2) (see column 4, lines 18-52). It was well known in the art at the time the present invention was made to use phase-locked loops to perform the same functions. Patel et al. disclose in Fig. 5, a digitally-controlled oscillator (270) which in combination with quadrature synchronous detector 250 forms a phase-locked loop using sine and cosine lookup tables (271 and 272) to generate sine and cosine function outputs at the same frequency as, and phase aligned with a quadrature-phased pair of input signals. In the embodiment of Fig. 5, Patel et al. include a second pair of sine and cosine lookup tables (2701 and 2702) for providing phase-adjusted sine and cosine signals to in-phase synchronous detector 230 to compensate for the delay introduced into the carrier signals by bandpass filters 52 and 53. It was well known in the digital signal processing art at the time the present invention was made to obtain synchronized harmonically-related signals from lookup tables by either multiplying the lookup address/index into one table by a constant (modulo the number of samples per period) to form a second index into the same or an identical table for generating a higher frequency waveform, or by providing a second lookup table having multiple periods of

the desired waveform stored in the same number of samples as a single period of a lower-frequency waveform stored in a first table. Whikehart et al. describes at column 2, line 63 –column 3, line 55, both of these methods for obtaining different harmonically-related sinusoidal signals. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to substitute the phase-locked loop of Patel et al. for circuit 21 of Figs. 1 and 2 of Vogt et al., with look-up tables 2701 and 2702 modified to store two cycles of the sine and cosine waveforms in the same number of samples as single cycles are stored in look-up tables 271 and 272, or alternatively, to multiply the indices into look-up tables 2701 and 2702 (a resultant phase value) by two (a predetermined positive integer), to produce a pair of phase-adjusted output signals synchronized at twice the frequency of the input quadrature-phased signals, producing sine(2*θ + α) and cosine(2*θ + α) lookup table outputs as an alternative to the circuit (21) disclosed by Vogt et al. in order to avoid the prior art.

27. Regarding claim 15, as indicated above regarding claim 1, Vogt et al. does not disclose a first decimator reducing the sampling rate of a first filter output as claimed in claim 1. Reich teaches decimating various signals to adapt the sampling rate to the maximum useful signal frequency to be processed. Fig. 1 of Reich shows decimating the baseband sum channel signal by a factor of three at d2 (from an initial sampling rate of 228 kS/s to 76 kS/s – see column 1, line 49 –column 2, line 11). What decimation factor is practical depends directly upon the sampling rate input to the decimator, which is not specified in the claims of the present invention. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to decimate the signals to whatever degree practical while maintaining the required intelligence depending upon the unspecified initial sampling rate.

Response to Arguments

28. Applicant's arguments with respect to claims 1, 18, 21, and 25 (and the associated dependent claims) have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

29. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

30. Simeau (US 4,208,547), Takahashi (4,029,906), and Sugai et al. (US 4,761,814) disclose decoders that apply separate and independent bandwidth control to sum and difference signals in response to decreased reception signal quality.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tony M Jacobson whose telephone number is 703-305-5532. The examiner can normally be reached on M-F 11:00-7:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forester W Isen can be reached on 703-305-4386. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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tmj

June 28, 2004

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PRIMARY EXAMINER